SEMICONDUCTOR DEVICE WITH LOW-K SPACERS

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] Generally, the present disclosure relates to the manufacture of sophisticated semiconductor devices, and, more specifically, to various methods of forming a semiconductor device with low-k spacers and various semiconductor devices incorporating such low-k spacers.

[0003] 2. Description of the Related Art

[0004] The fabrication of advanced integrated circuits, such as CPU's, storage devices, ASIC's (application specific integrated circuits) and the like, requires the formation of a large number of circuit elements in a given chip area according to a specified circuit layout. Field effect transistors (NMOS and PMOS transistors) represent one important type of circuit element that substantially determines performance of such integrated circuits. During the fabrication of complex integrated circuits using, for instance, MOS technology, millions of transistors, e.g., NFET transistors and/or PFET transistors, are formed on a substrate including a crystalline semiconductor layer. A field effect transistor, whether an NFET or a PFET device, is a planar device that typically includes a source region, a drain region, a channel region that is positioned between the source region and the drain region, a gate insulation layer and a gate electrode positioned above the gate insulation layer over the channel region. By applying an appropriate voltage to the gate electrode, the channel region becomes conductive and current is allowed to flow from the source region to the drain region.

[0005] For many early device technology generations, the gate structures of most transistor elements has been comprised of a plurality of silicon-based materials, such as a silicon dioxide and/or silicon oxynitride gate insulation layer, in combination with a polysilicon gate electrode. However, as the channel length of aggressively scaled transistor elements has become increasingly smaller, many newer generation devices employ gate structures that contain alternative materials in an effort to avoid the short channel effects which may be associated with the use of traditional silicon-based materials in reduced channel length transistors. For example, in some aggressively scaled transistor elements, which may have channel lengths on the order of approximately 10-20 nm or less, gate structures that include a so-called high-k dielectric gate insulation layer and one or metal layers that function as the gate electrode (HK/MG) have been implemented. Such alternative gate structures have been shown to provide significantly enhanced operational characteristics over the heretofore more traditional silicon dioxide/polysilicon gate structure configurations.

[0006] Depending on the specific overall device requirements, several different high-k materials—i.e., materials having a dielectric constant, or k-value, of approximately 10 or greater—have been used with varying degrees of success for the gate insulation layer in an HK/MG gate electrode structure. For example, in some transistor element designs, a high-k gate insulation layer may include tantalum oxide (Ta_2O_5), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), titanium oxide (TiO_2), aluminum oxide (Al_2O_3), hafnium silicates ($HfSiO_x$) and the like. Furthermore, one or more non-polysilicon metal gate electrode materials—i.e., a metal gate stack—may be used in HK/MG configurations so as to control the work function of the transistor. These metal gate electrode materials may include, for example, one or more layers of titanium (Ti), titanium nitride (TiN), titanium-aluminum (TiAl), aluminum (Al), aluminum nitride (AlN), tantalum (Ta), tantalum nitride (TaN), tantalum carbide (TaC), tantalum carbonitride (TaCN), tantalum silicon nitride (TaSiN), tantalum silicide (TaSi) and the like.

[0007] One well-known processing method that has been used for forming a transistor with a high-k/metal gate structure is the so-called "gate last" or "replacement gate" technique. FIGS. **1**A-**1**D depict one illustrative prior art method for forming an HK/MG replacement gate structure using a gate last technique. As shown in FIG. **1**A, the process includes the formation of a basic transistor structure **200** above a semiconducting substrate **210** in an active area defined by a shallow trench isolation structure **211**. At the point of fabrication depicted in FIG. **1**A, the device **200** includes a sacrificial gate insulation layer **212**, a dummy or sacrificial gate electrode **214**, sidewall spacers **216**, a layer of insulating material **217** and source/drain regions **218** formed in the substrate **210**. The various components and structures of the device **200** may be formed using a variety of different materials and by performing a variety of known techniques. For example, the sacrificial gate insulation layer **212** may be comprised of silicon dioxide, the sacrificial gate electrode **214** may be comprised of polysilicon, the sidewall spacers **216** may be comprised of silicon nitride and the layer of insulating material **217** may be comprised of silicon dioxide. The source/drain regions **218** may be comprised of implanted dopant materials (N-type dopants for NFET devices and P-type dopants for PFET devices) that are implanted into the substrate **210** using known masking and ion implantation techniques. Of course, those skilled in the art will recognize that there are other features of the transistor **200** that are not depicted in the drawings for purposes of clarity. For example, so-called halo implant regions are not depicted in the drawings, as well as various layers or regions of silicon/germanium that are typically found in high performance PFET transistors. At the point of fabrication depicted in FIG. **1**A, the various structures of the device **200** have been formed and a chemical mechanical polishing process (CMP) has been performed to remove any materials above the sacrificial gate electrode **214** (such as a protective cap layer (not shown) comprised of silicon nitride) so that at least the sacrificial gate electrode **214** may be removed.

[0008] As shown in FIG. **1**B, one or more etching processes are performed to remove the sacrificial gate electrode **214** and the sacrificial gate insulation layer **212** to thereby define a gate cavity **220** where a replacement gate structure will subsequently be formed. A masking layer that is typically used in such etching processes is not depicted for purposes of clarity. Typically, the sacrificial gate insulation layer **212** is removed as part of the replacement gate technique, as depicted herein. However, the sacrificial gate insulation layer **212** may not be removed in all applications.

[0009] Next, as shown in FIG. **1**C, various layers of material that will constitute a replacement gate structure **230** are formed in the gate cavity **220**. The materials used for such replacement gate structures **230** may vary depending upon the particular application. Even in cases where the sacrificial gate insulation layer **212** is intentionally removed, there will typically be a very thin native oxide layer (not shown) that forms on the substrate **210** within the gate cavity **220**. In one illustrative example, the replacement gate structure **230** is comprised of a high-k gate insulation layer **230**A, such as hafnium